REMARKS

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Related Art FIGs. 2 and 3F (hereinafter "APAF") in view of U.S. Patent No. 5,162,933 (hereinafter "Kakuda"). Applicant respectfully traverses the rejection as being based upon Applicant's Related Art and a reference that neither teach nor suggest the novel combination of features recited by independent claim 1, and hence dependent claims 2-14.

With respect to independent claim 1, as amended, Applicant respectfully submits that neither of APAF nor Kakuda disclose a claimed combination comprising at least feature of "a plurality of thin film transistors formed on the substrate adjacent to intersections of the gate lines and the data lines, each thin film transistor including a gate electrode, a gate insulation layer, an active layer, an ohmic contact layer, a source electrode, and a drain electrode, the source electrode extended from each of the data lines and overlapping a portion of the gate electrode" and "wherein the source electrode is positioned between the ohmic contact layer and the metal layer."

The Office Action admits that Applicant's Related Art FIGs. 2 and 3F discloses all the features of claim 1, "except the metal layer formed on an entire surface of each of the data line and the source electrode." Accordingly, the Office Action relies upon Kakuda for allegedly showing "an LCD device having a data line 11 with a metal layer formed on the entire surface." In addition, the Office Action alleges that "a source electrode (22) extends from the data line (col. 4, lines 50-53) and is covered with a metal layer (11b in fig. 4). Applicant respectfully disagrees.

In figure 4 of Kakuda, a semiconductor layer (24) should be formed on a portion of the source electrode (22). The semiconductor layer (24) should bridge across a gap between the source and drain electrodes 22 and 23 (col. 4, lines 53-55). Accordingly, it is impossible for the

metal layer (11b) to be formed on an entire surface of the source electrode (22).

Moreover, in figure 4 of Kakuda, a metal layer (11b) is positioned on a lower layer (11a) of the data line (11), and the source electrode (22) extends from the lower layer (11a). The semiconductor layer (24) is positioned on the source electrode (22). Among the metal layer 11b, the lower layer (11a) and the source electrode (22), the source electrode (22) is a lowest layer. Accordingly, Kakuda fails to disclose the feature of "the source electrode is positioned between the ohmic contact layer and the metal layer" in claim 1.

For at least the above reasons, Applicants respectfully submit that claims 1-14 are neither taught nor suggested by APAF and/or Kakuda, whether taken alone or in combination. Thus, Applicant respectfully asserts that the rejections under 35 U.S.C. § 103(a) should be withdrawn because the above-discussed novel combination of features are neither taught nor suggested by any of the applied references.

Conclusion

In view of the foregoing, Applicant respectfully requests reconsideration and timely allowance of the pending claims. Should the Examiner believe that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under

37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,
Morgan, Lewis & Bockius LLP

Dated: May 27, 2008 By: _____
Robert J. Goodell, Reg. No. 41,040

Customer No. 009629
Morgan, Lewis & Bockius LLP
1111 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
Tel: 202-739-3000
Fax: 202-739-3001